CLAIMS

1. An error detection apparatus having a syndrome operator for performing syndrome operation to target code strings, each target code string comprising plural sectors and each sector comprising matrix data, and performing an error correction processing by an error correction circuit to the target code strings, and simultaneously, performing error detection to the target code strings in sector units, said apparatus comprising:

an error detection code operation circuit for calculating error detection codes in the target code strings;

an error detection code skip operation circuit for, when the target code strings are inputted in a discontinuous arrangement, performing a skip operation for correcting the inter-data continuity by skipping the data so as to make the arrangement of the code strings continuous;

a first error detection control circuit for controlling a first error detection code operation performed by the error detection code operation circuit or the error detection code skip operation circuit, which is carried out simultaneously with the syndrome operation;

a second error detection control circuit for controlling, after the error correction processing, a second error detection code operation only for data indicated by error data position on the basis of the error data positions and error data numeral

values that are obtained by the error correction processing, and controlling an updation processing for updating the operation result of the first error detection code operation on the basis of the operation result of the second error detection code operation; and

a memory for holding the operation results by the error detection code operation circuit, and the error detection code skip operation circuit.

2. An error detection apparatus as defined in Claim 1 wherein said error detection code skip operation circuit receives error detection codes of target code strings which have been inputted by the last time, and performs a skip operation which has previously been set in the error detection code skip operation circuit.

3. An error detection apparatus as defined in Claim 1 wherein said memory comprises

a first memory for holding the per-sector operation results by the error detection code operation circuit and the error detection code skip operation circuit when the target code strings are inputted in a continuous arrangement, and holding the halfway operation results for each sector by the error detection code operation circuit and the error detection code skip operation circuit when the target code strings are inputted in a

discontinuous arrangement; and

a second memory for holding the operation results transmitted from the first memory, for each sector.

4. An error detection apparatus as defined in Claim 1 wherein said first memory comprises a memory for holding the operation result by the first error detection code operation which is executed by the error detection code operation circuit and the error detection code skip operation circuit, and a memory for holding a difference operation result by the second error detection code operation, for updating the operation result of the first error detection code operation.

5. An error detection apparatus as defined in Claim 1 wherein, when the target code strings are inputted in a discontinuous arrangement, said error detection code skip operation circuit performs a skip operation for skipping a predetermined number of bytes in non-final rows in the sector among the target code strings, and performs an individual skip operation for skipping a number of bytes according to column positions where data exist, in a final row in the sector among the target code strings.

6. An error detection apparatus as defined in Claim 1 further comprising a scramble removal unit for collectively removing scramble components in the target code strings.

7. An error detection apparatus as defined in Claim 6 wherein said scramble removal unit includes a table which holds data for removing scramble components in the target code strings.

8. An error detection method for performing error correction in units of error correction unit blocks for target code strings inputted in a discontinuous arrangement, each target code string being constituted by plural sectors each comprising matrix data, and simultaneously, performing error detection in sector units for the target code strings inputted in a discontinuous arrangement, said method comprising:

a syndrome operation step of performing a syndrome operation to the target code strings;

a first error detection code operation step of performing an error detection code operation to the target code strings inputted in a discontinuous arrangement, which is performed simultaneously with the syndrome operation step;

an error correction step of performing error correction by calculating error data positions and error data numeral values of the target code strings, on the basis of the syndrome obtained in the syndrome operation step;

a second error detection code operation step of performing an error detection code operation again to only data in the error data positions among the target code strings, on the basis of the

error data positions and the error data numeral values which are obtained in the error correction step; and

an updation step of updating the operation result by the first error detection code operation step, using the operation result by the second error detection code operation step; and

each of said first error detection code operation step and the second error detection code operation step including an error detection code operation step of calculating error detection codes in the target code strings, and an error detection code skip operation step of performing a skip operation for correcting the inter-data continuity by skipping the data so as to continuously arranging the target code strings which are inputted in a discontinuous arrangement.

9. An error detection method as defined in Claim 8 wherein said error detection code skip operation step receives error detection codes of target code strings which have been inputted by the last time, and performs a skip operation which has previously been set.

10. An error detection method as defined in Claim 8 wherein said error detection code skip operation step comprises performing a skip operation for skipping a predetermined number of bytes in non-final rows in the sector among the target code strings, and performing an individual skip operation for skipping a number of bytes according to column positions where data exist, in a final

row in the sector among the target code strings.

11. An error detection method as defined in Claim 10 wherein said individual skip operation is carried out by utilizing plural times the operation result of the skip operation that is executed in a specific column position among the column positions where data exist.

12. An error detection method as defined in Claim 8 further comprising a scramble removal step of removing scramble components included in the target code strings, which is carried out simultaneously with the updation step.

13. An error detection method as defined in Claim 12 wherein, after all data in one sector are inputted, said scramble removal step removes scramble components in the all data in the sector collectively.

14. An error detection method as defined in Claim 12 wherein said scramble removal step is carried out using a table which holds data for removing scramble components in the target code strings.